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(54) **METHOD FOR MANUFACTURING CONTACT
 HOLE OF SEMICONDUCTOR DEVICE**

(57) Abstract:

PROBLEM TO BE SOLVED: To prevent a gate that is adjacent to a conductive region being exposed by a contact hole and a silicide being formed on the gate from being exposed by performing a vertical etching process using an etching barrier pattern for limiting the contact hole to the minimum size.

SOLUTION: First and second etching barrier film patterns 140P and 142P are formed on a lower interlayer insulation film 130. Then, a first contact hole for exposing a first conductive region 113 is formed by the first etching barrier film pattern 140P. Then, after a conductive film pattern for burying the first contact hole is formed, an upper interlayer insulation film 180 is formed on an entire surface. Then, the lower interlayer insulation film 130 is etched by the second etching barrier film pattern 142P being exposed by the etched upper interlayer insulation film 180, a fourth contact hole 190 consisting of a third

contact hole through the upper interlayer insulation film 180 and a second contact hole through the lower interlayer insulation film 130 is formed.

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